METHOD FOR OPTIMIZING DECOUPLING CAPACITOR DESIGN IN DELAY LOCKED LOOPS

Abstract

A method for optimizing decoupling capacitance in a delay locked loop is provided. A representative power supply waveform having noise is input into a simulation of the delay locked loop; an estimate of jitter is determined; and an amount of the decoupling capacitance is adjusted until the jitter falls below a pre-selected value. Further, a computer system for optimizing decoupling capacitance in a delay locked loop is provided. Further, a computer-readable medium having recorded thereon instructions adapted to optimize decoupling capacitance in a delay locked loop is provided.

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